

FIG. 1A

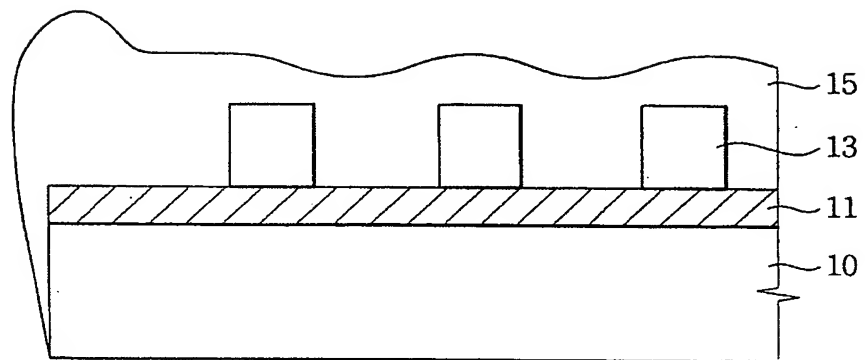


FIG. 1B

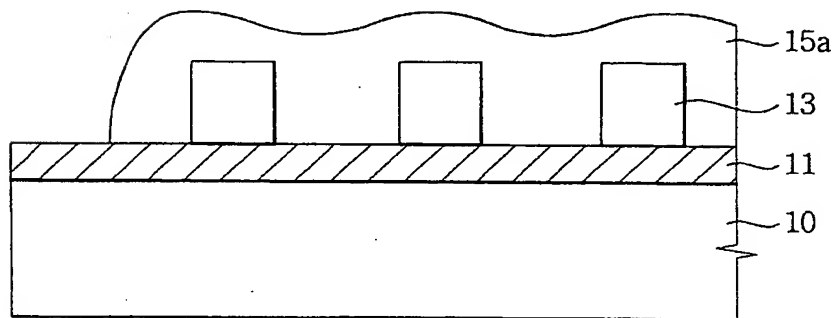


FIG.2

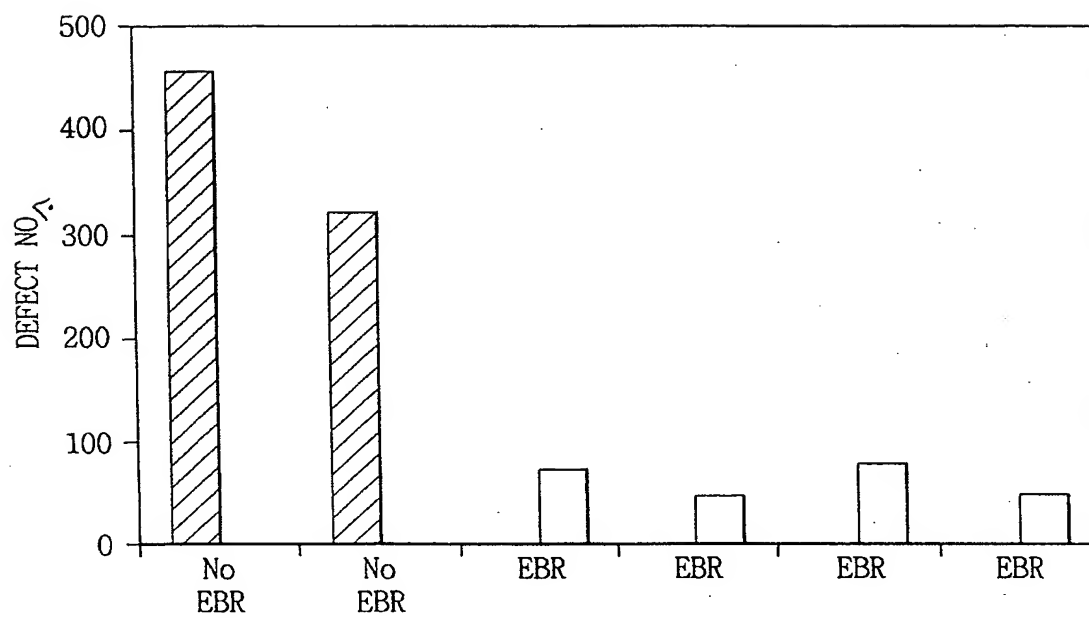


FIG.3

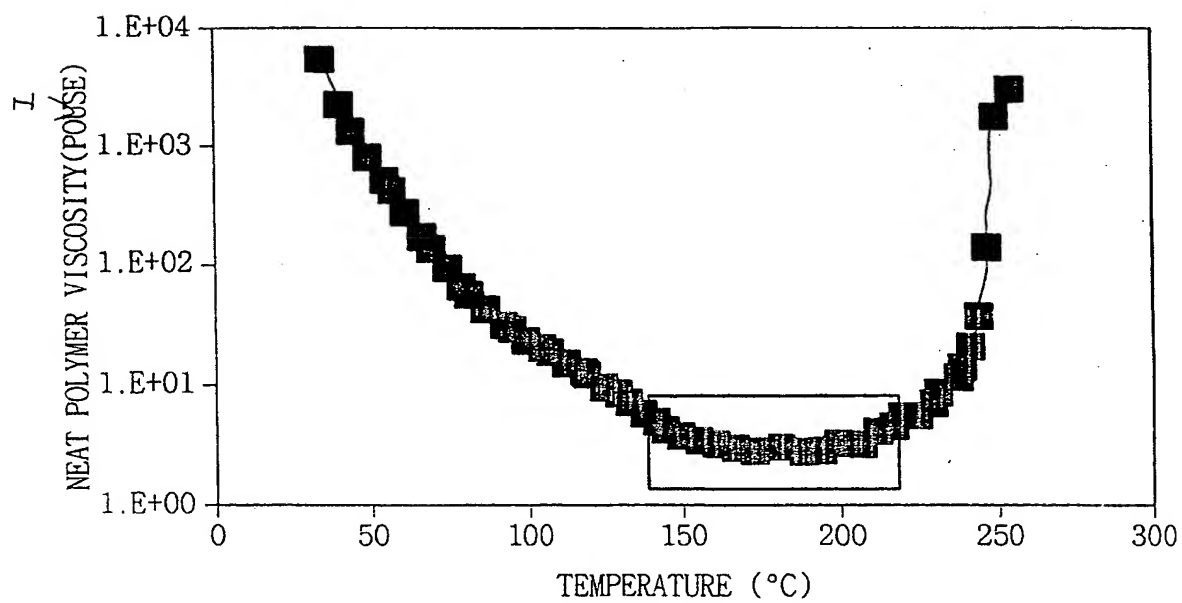


FIG. 4A

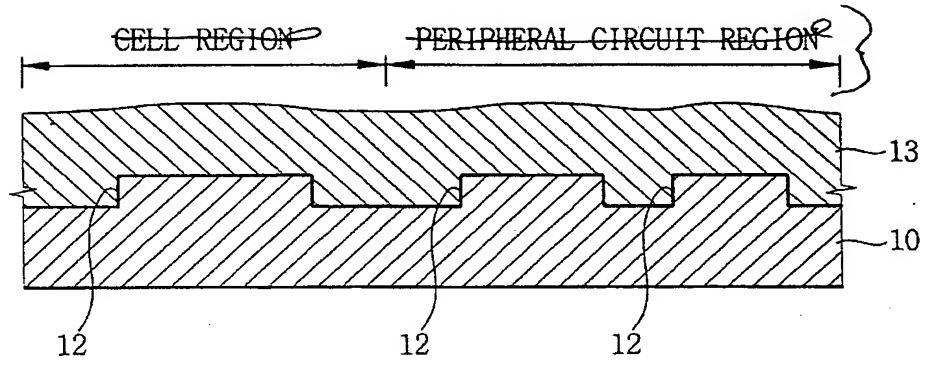


FIG. 4B

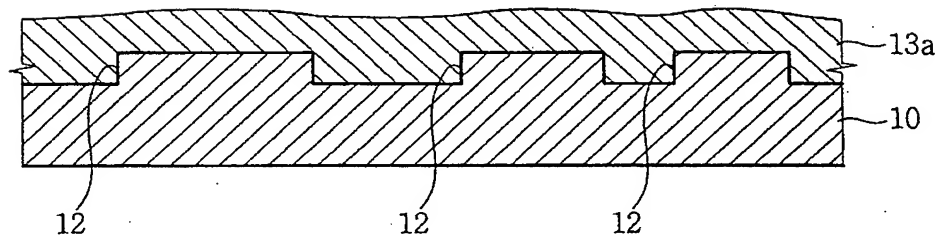


FIG. 4C

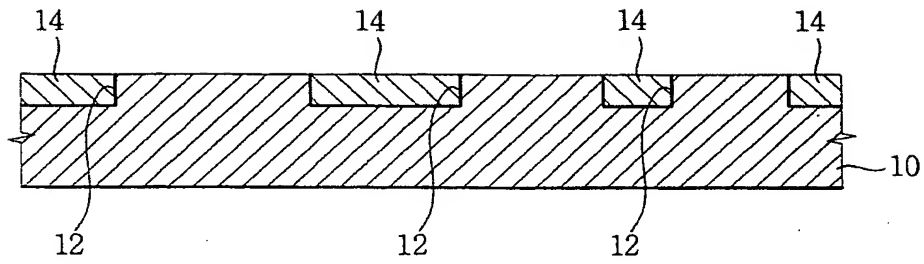


FIG. 4D

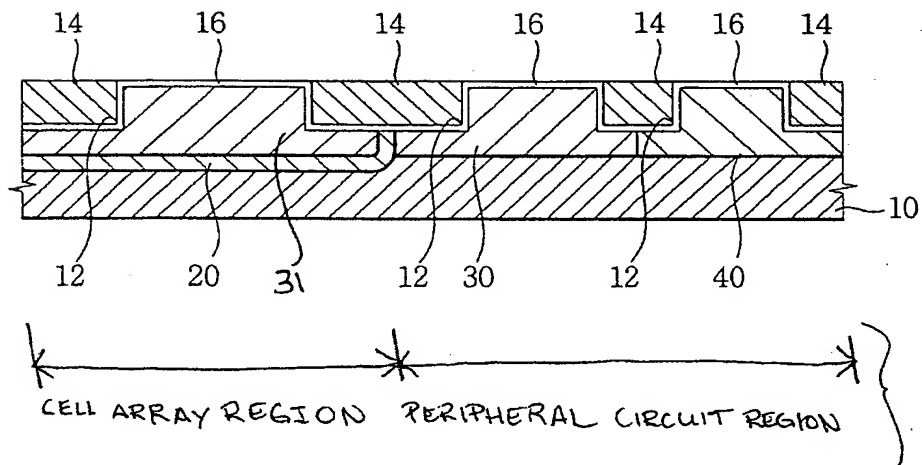


FIG. 4E

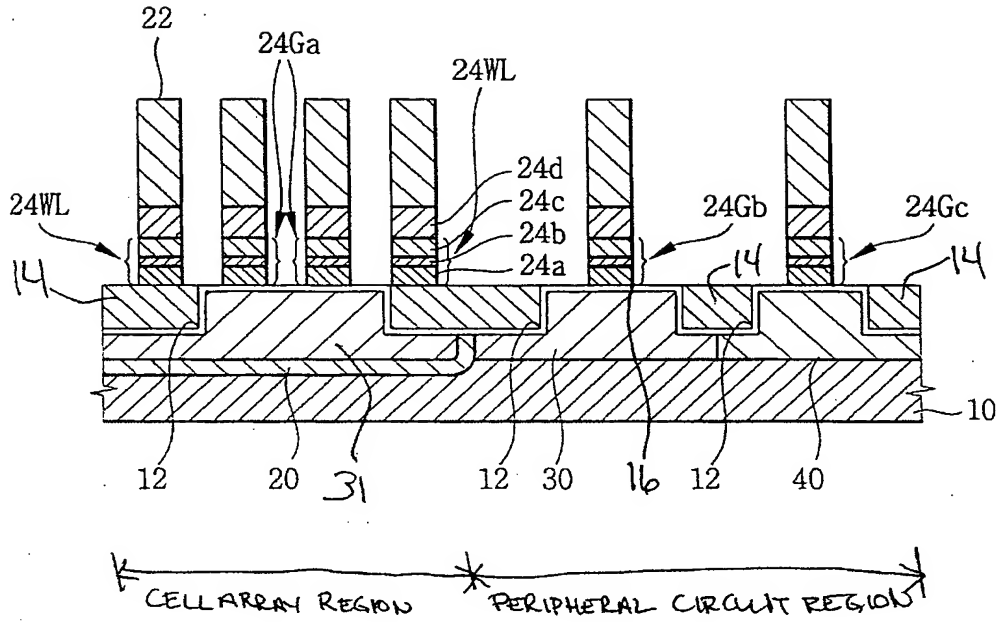
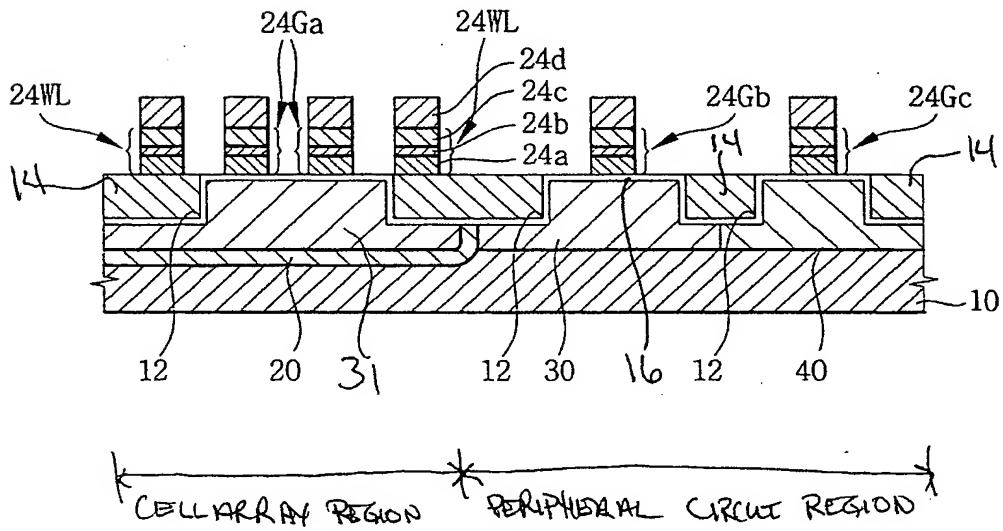


FIG. 4F



A detailed cross-sectional view of a semiconductor device, divided into two main functional areas: a **CELLULAR ARRAY REGION** on the left and a **PERIPHERAL CIRCUIT REGION** on the right, separated by a vertical dashed line.

CELLULAR ARRAY REGION: This region contains a series of repeating unit cells. Each unit cell consists of a vertical stack of layers: a bottom layer (12), a middle layer (26), and a top layer (20). The top layer (20) is patterned into a grid of rectangular blocks. The blocks are interconnected by horizontal lines (26) and vertical lines (32). The top surface of the blocks is labeled 24WL. The bottom surface of the blocks is labeled 24Ga. The bottom surface of the vertical lines is labeled 24WL. The bottom surface of the horizontal lines is labeled 24Gc.

PERIPHERAL CIRCUIT REGION: This region contains larger, more complex structures. It includes a large rectangular block (32a) and a smaller rectangular block (42e). The large block (32a) is connected to a horizontal line (30) and a vertical line (27). The smaller block (42e) is connected to a horizontal line (40) and a vertical line (25). The bottom surface of the large block is labeled 24Gb. The bottom surface of the smaller block is labeled 24Gc. The bottom surface of the horizontal lines is labeled 24Gc. The bottom surface of the vertical lines is labeled 24WL.

The entire device is built on a substrate (10). The bottom surface of the substrate is labeled 10. The top surface of the substrate is labeled 12. The bottom surface of the substrate is labeled 10. The top surface of the substrate is labeled 12.

This diagram is a cross-sectional view of a semiconductor device, divided into two main functional areas: a memory array region and a peripheral circuit region.

- Memory Array Region (Left):** This region contains a series of memory cells. Each cell consists of a vertical stack of layers: a bottom layer (12), a middle layer (26), and a top layer (20). The cells are separated by vertical spacers (26). The top surface of the array is labeled 24WL, indicating word lines.
- Peripheral Circuit Region (Right):** This region contains peripheral circuitry. It features a series of vertical stacks (32a, 32b, 32c) and a central stack (32d). The top surface of this region is labeled 24Ga, indicating gate lines. The peripheral circuitry is separated from the array region by a vertical boundary (30).
- Common Layers:** The device has a common bottom layer (10) and a common top layer (50) that span both the array and peripheral regions.

FIG. 4I

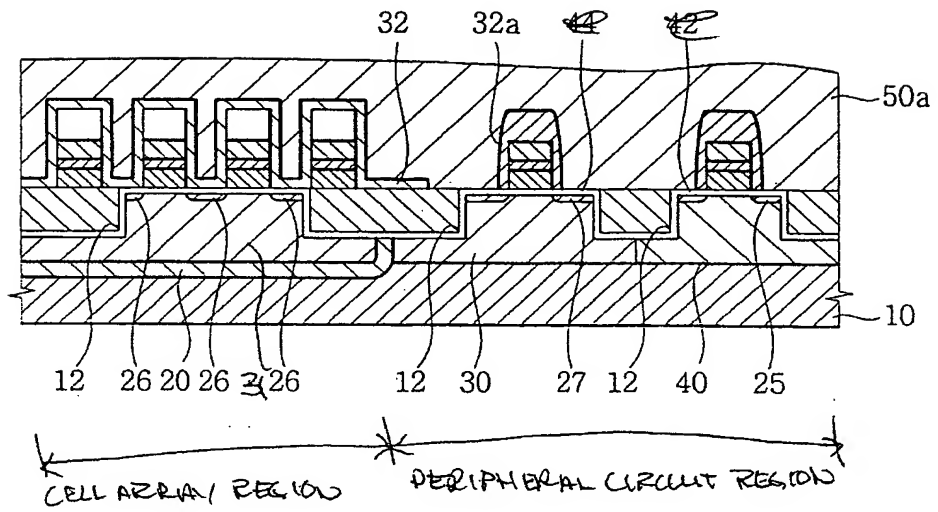


FIG. 4J

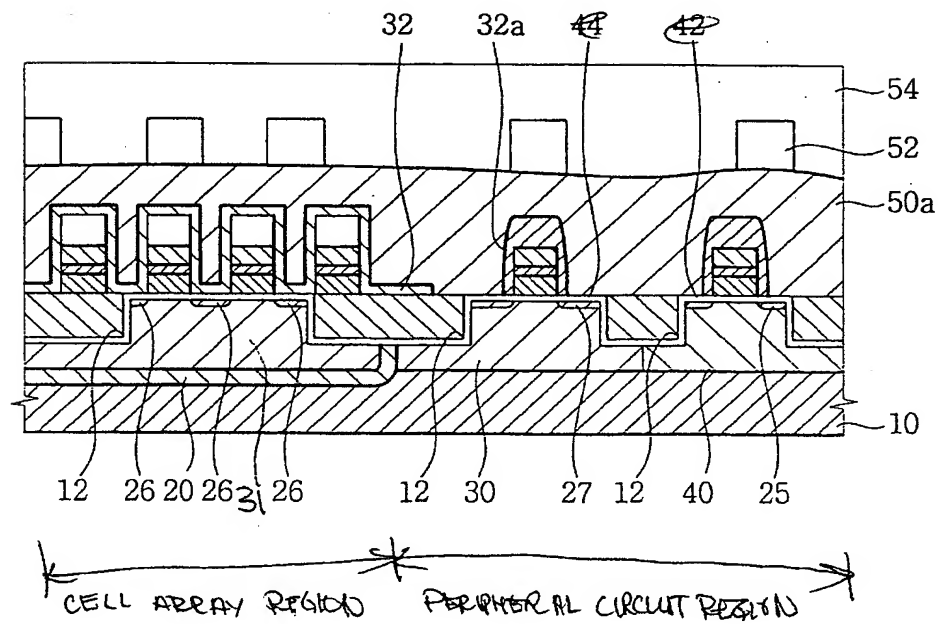


FIG. 4K

